

## システム情報工学研究科修士論文概要

年 度	平成 26 年度	学位名		修士(工学)
専 攻	知能機能システム	専攻	著者氏名	Block Saldana, Henry Jose
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論文題目				
An FPGA Hardware Acceleration of a Phylogenetic Tree Reconstruction with Maximum Parsimony Algorithm (FPGA を用いた最節約法による進化系統樹の高速計算)				
論文概要				
<p>In this work, we present an FPGA hardware implementation for a phylogenetic tree reconstruction with maximum parsimony algorithm. We base our approach on a particular stochastic local search algorithm that uses the Indirect Calculation of Tree Lengths method and the Progressive Neighborhood. In our implementation, we define a tree structure, and accelerate the search by parallel and pipeline processing. We show results for eight real-world biological datasets. We compare execution times against another hardware approach, and TNT, the fastest available parsimony program. Acceleration rates between 34 to 45 per rearrangement, and 2 to 6, for the whole search, are obtained against the other hardware approach. Acceleration rates between 2 to 36 per rearrangement, and 18 to 112, for the whole search, are obtained against TNT. We estimate that these acceleration rates could increase for even larger datasets.</p>				
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